What I claim is:

1. A multi-chip package type semiconductor device, comprising:

an insulating substrate having thereon a first conductive pattern and a second conductive pattern;

a first semiconductor chip having a first internal circuit on the insulating substrate, the first semiconductor chip having a first terminal pad connecting to the first internal circuit and a conductive relay pad isolated from the first terminal pad, and the conductive relay pad including a first area and a second area;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a second internal circuit and having a second terminal pad connecting to the second internal circuit;

a first bonding wire connecting the first terminal pad to the first conductive pattern;

a second bonding wire connecting the second conductive pattern to the conductive relay pad in the first area; and

a third bonding wire connecting the conductive relay pad in the second area to the second terminal pad;

wherein the lengths of the first, second and third bonding wire are approximately the same.

2. A multi-chip package type semiconductor device, as claimed in claim 1,

wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

3. A multi-chip package type semiconductor device, as claimed in claim 2, further comprising a first metal bump formed on the conductive relay pad in the first area and a second metal bump formed on the second terminal pad, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the second conductive pattern and the second bond as the ending connection of the second bonding wire is made at the first metal bump, and wherein the first bond as the beginning connection of the third bonding wire is preformed at the conductive relay pad in the second area and the second bond as the ending connection of the third bonding wire is made at the second metal bump.

4. A multi-chip package type semiconductor device, as claimed in claim 2, further comprising a metal bump formed on the conductive relay pad in the second area, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the

conductive relay pad in the first area and the second bond as the ending connection of the second bonding wire is made at the second conductive pattern, and wherein the first bond as the beginning connection of the third bonding wire is preformed at the second terminal pad and the second bond as the ending connection of the third bonding wire is made at the metal bump.

5. A multi-chip package type semiconductor device, as claimed in claim 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on the periphery of the first semiconductor chip, and the longer side of the rectangularly-shaped conductive relay pad is parallel to the side of the first semiconductor chip.

6. A multi-chip package type semiconductor device, as claimed in claim 3, wherein the conductive relay pad is rectangularly-shaped, and is formed on the periphery of the first semiconductor chip, and the shorter side of the rectangularly-shaped conductive relay pad is parallel to the side of the first semiconductor chip.

7. A multi-chip package type semiconductor device, as claimed in claim 6, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

8. A multi-chip package type semiconductor device, as claimed in claim 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on the

periphery of the first semiconductor chip, and the longer side of the rectangularly-shaped conductive relay pad is parallel to the side of the first semiconductor chip.

9. A multi-chip package type semiconductor device, as claimed in claim 4, wherein the conductive relay pad is rectangularly-shaped, and is formed on the periphery of the first semiconductor chip, and the shorter side of the rectangularly-shaped conductive relay pad is parallel to the side of the first semiconductor chip.

10. A multi-chip package type semiconductor device, as claimed in claim 9, wherein the first area of the rectangularly-shaped conductive relay pad is closer to the side of the first semiconductor chip than the second area.

11. A multi-chip package type semiconductor device, as claimed in claim 3, wherein the first metal bump is not physically connected to the first bond of the third bonding wire, but is electrically connected to the first bond of the third bonding wire via the conductive relay pad.

12. A multi-chip package type semiconductor device, as claimed in claim 4, wherein the metal bump is not physically connected to the first bond of the second bonding wire, but is electrically connected to the first bond of the second bonding wire via the conductive relay pad.

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13. A multi-chip package type semiconductor device, comprising:

a first semiconductor chip having a first terminal and a conductive relay pad, the conductive relay pad including a first area and a second area;

a second semiconductor chip, which is placed on the first semiconductor chip, the second semiconductor chip having a second terminal pad, connected to the conductive relay pad in the second area;

a first internal terminal connected to the first terminal pad; and

a second internal terminal connected to the conductive relay pad in the first area.

14. A multi-chip package type semiconductor device, as claimed in claim 13, further comprising an insulating substrate, wherein the first and second internal terminals are formed on the insulating substrate, and the first semiconductor chip is placed on the insulating substrate.

15. A multi-chip package type semiconductor device, comprising:

an insulating substrate having a first and second conductive patterns thereon;

a first semiconductor chip on the insulating substrate, the first semiconductor chip having a first internal circuit, a first terminal pad connecting to the first internal circuit and a conductive relay pad isolated from the first terminal pad;

a second semiconductor chip on the first semiconductor chip, the second semiconductor chip being smaller than the first semiconductor chip, and having a

second internal circuit and having a second terminal pad connecting to the second internal circuit;

a first bonding wire connecting the first terminal pad to the first conductive pattern;

a second bonding wire connecting the second conductive pattern to the conductive relay pad; and

a third bonding wire connecting the conductive relay pad to the second terminal pad;

wherein the lengths of the first, second and third bonding wire are approximately the same.

16. A multi-chip package type semiconductor device, as claimed in claim 15, wherein the second semiconductor chip is placed on the center of the first semiconductor chip.

17. A multi-chip package type semiconductor device, as claimed in claim 16, further comprising a first metal bump formed on the conductive relay pad and a second metal bump formed on the second terminal pad, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the second conductive

pattern and the second bond as the ending connection of the second bonding wire is made at the first metal bump, and wherein the first bond as the beginning connection of the third bonding wire is preformed at the first metal bump and the second bond as the ending connection of the third bonding wire is made at the second metal bump.

18. A multi-chip package type semiconductor device, as claimed in claim 16, further comprising a metal bump formed on the conductive relay pad, wherein the first bond as the beginning connection of the first bonding wire is preformed at the first terminal pad and the second bond as the ending connection of the first bonding wire is made at the first conductive pattern, wherein the first bond as the beginning connection of the second bonding wire is preformed at the conductive pattern and the second bond as the ending connection of the second bonding wire is made at the metal bump, and wherein the first bond as the beginning connection of the third bonding wire is preformed at the second terminal pad and the second bond as the ending connection of the third bonding wire is made at the metal bump.

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